Stanford AHA Agile Hardware Center and Affiliates Program

AHA Vision

The Stanford AHA Agile Hardware Center is a Stanford University research center and industrial affiliates program. AHA will develop technologies that enable designers to easily create and add powerful feature-rich applications, computing, and communications to any intelligent device or system. This vision requires custom application- specific accelerators and agile system and hardware development tools.

AHA Team

The AHA team consists of six Stanford professors and their research groups:

Clark Barrett, Computer Science: Satisfiability, formal software and hardware verification, and automated reasoning.

Kayvon Fatahalian, Computer Science: Architecture of high-performance visual computing systems, specifically visual data analysis engine, and graphics engine compiler.

Pat Hanrahan, Computer Science and Electrical Engineering: Visualization and scientific illustration, graphics systems and architectures including a programming environment for GPUs, and rendering algorithms for natural environments.

Mark Horowitz, Electrical Engineering and Computer Science: New design methodologies for VLSI circuits including analog and digital design methods, low-energy processors, and computational photography.

Fredrik Kjolstad, Computer Science: Compilers and programming models, specifically programming systems for sparse computing applications.

Priyanka Raina, Electrical Engineering: Design of energy-efficient circuits and systems for demanding applications on constrained-resource devices such as accelerating multimedia applications on mobile devices.

Philosophy

Hardware and software systems must become easier and more fun to develop. The AHA team aims to enable a more agile hardware development flow to quickly and easily modify an existing design. Design, validation, and software are now the critical issues. Solving these issues requires expertise in the application area and hardware design. The AHA team uses agile design practices and continuous integration with rapid design cycles and frequent tapeouts. The team uses their own tools to create prototypes, and uses their own prototypes to create new systems.

Research Themes

The AHA Agile Hardware Project consists of three components:

1) Tool Chain. To support agile practices, the research will create a new tool chain for design and testing of unified hardware and software systems optimized for rapid design iteration.
2) Coarse Grain Reconfigurable SoC. To further simplify the hardware design process, the research will create an SoC combining open source Linux with RISC-V cores and a CGRA that is optimized for image processing.
3) Improved SMT Solvers. From high-level validation to optimization to layout, agility requires replacing manual efforts with efficient automated tools wherever possible. AHA research aims to dramatically improve upon the performance of current SMT (satisfiability modulo theory) solvers for hardware analysis and add capabilities for optimization.

The AHA team is using intelligent processing of rich video streams as an exemplary problem and driving application for research. This includes machine learning and multi-modal video. It spans a wide range of resources and environments from mobile to cloud. The AHA projects include the following elements:

- Improved video analysis algorithms
- Improved Halide compiler including auto-scheduler, hardware backend, and driver/glue software generation
- Open source tool chain for compiling hardware
- Parameterized SoC generator including RISC-V host cores and AHA's own coarse-grained reconfigurable architecture (CGRA)
- Formal methods for hardware validation and better SMT solvers

Video Analysis

TASK	APPLICATIONS
Cloud-scale video data mining	Image processing and DNN inference on millions of hours of video, offline training on video collections
Real-time video stream and multi-stream processing	Computational photography, autonomous vehicles, VR
Low latency, ultra-low power deployments	Always-on sensing / wakeboarding, sense / process / display

Halide Compiler

TASK	APPLICATIONS
Auto schedulers	For Halide and Halide intermediate representation (IR)
Generating hardware from Halide	Line-buffered pipelines, dense linear algebra (xNN), system glue to connect to user applications
Framework extensions	More-dynamic applications

Engagement

The AHA Center brings together diverse funding sources including Intel Science and Technology Centers for Visual Cloud and Agile Hardware, DARPA research grants, and an industrial affiliates program. Members of the affiliates program are an integral part of AHA. They provide insights on real-world problems, opportunities, and constraints that inform and inspire AHA research. They engage with faculty and students. They provide a path to testing and applying our innovations, thus leading to large-scale impact.

Corporate engagement includes the following elements:

- Invitations to two technical retreats per year
- Invitations to monthly review meetings
- Invitations to on-campus seminars and workshops that are great opportunities to engage with students
- An opportunity to serve on the AHA advisory board, thus providing input on industry considerations
- Early and facilitated access to innovations including software, tools, and hardware prototypes that we develop, under a permissive open source license
- Access to faculty members and students to discuss research and pursue collaboration

Funding

Corporate members contribute $250,000 per year with the expectation of at least three years of membership. AHA is a Stanford University industrial affiliates program and is subject to university policies for such programs including openness in research, publication and broad sharing of results, and faculty freedom to pursue research topics and methodology of their choice. See https://industrialaffiliates.stanford.edu/ .

IP

AHA researchers will use and develop open-source software, and it is the intention of all AHA researchers that any software released will be released under an open source model, such as BSD.

Information

For further information please contact Mark Horowitz at horowitz@ee.stanford.edu.